## Amendments to the Claims

The following Listing of Claims replaces all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-38 (canceled)

Claim 39 (currently amended): An integrated circuit comprising:

a transistor level comprising one or more semiconductor devices disposed over a substrate and an overlying transistor isolation layer having at least one contact via extending therethrough;

a ferroelectric device level [[structure,]] positioned over the transistor isolation layer ~~, including, a ferroelectric device level, disposed over the transistor isolation layer~~, the ferroelectric device level including at least one ferroelectric capacitor and an [[,]] overlying ferroelectric isolation layer having at least one via extending therethrough and aligned with a corresponding contact via, the via extending through the ferroelectric isolation layer being laterally sized larger than the corresponding contact via aligned therewith; [[,]]

a first metal level [[layer]] disposed over the ferroelectric device level; [[, and]]

an inter-level dielectric level disposed over the first metal level; and

a second metal level disposed over the inter-level dielectric level.

Claim 40 (currently amended): An integrated circuit, as defined in claim 39, wherein each ~~the~~ contact via is ~~vias are~~ filled with a respective tungsten contact plug ~~plugs~~.

Claim 41 (currently amended): An integrated circuit, as defined in claim 40, wherein each ~~the~~ ferroelectric capacitor is ~~capacitors are~~ formed over a respective tungsten contact plug ~~plugs~~.

Claims 42-56 (canceled)

Claim 57 (currently amended): A method of forming an integrated comprising:

forming a transistor level comprising one or more semiconductor devices disposed over a substrate and an overlying transistor isolation layer having at least one contact via extending therethrough;

forming a ferroelectric device level over the transistor isolation layer, the ferroelectric layer including at least one ferroelectric capacitor and an overlying ferroelectric isolation layer having at least one via extending therethrough and aligned with a corresponding contact via, the via extending through the ferroelectric isolation layer being laterally sized larger than the corresponding contact via aligned therewith;

forming a first metal level [[layer]] over the ferroelectric device level;

forming an inter-level dielectric level over the first metal level; and [[layer;]]

forming a second metal level over the inter-level dielectric level [[; and]]

~~overlying ferroelectric isolation layer having at least one via extending therethrough, wherein the via being laterally sized larger than the corresponding contact via aligned therewith~~.

Claim 58 (currently amended): A method of forming an integrated circuit, as defined in claim 57, wherein each ~~the~~ contact via is ~~vias are~~ filled with a respective tungsten contact plug ~~plugs~~.

Claim 59 (currently amended): A method of forming an integrated circuit, as defined in claim 58, wherein the ferroelectric capacitor is ~~capacitors are~~ formed over a respective tungsten contact plug [[plugs]].

Claim 71 (new): An integrated circuit, as defined in claim 39, wherein between the ferroelectric device level and the transistor isolation layer is free of any interposing metal level.

Claim 72 (new): An integrated circuit, as defined in claim 39, wherein throughout the ferroelectric isolation layer each ferroelectric isolation layer via is laterally sized larger than the corresponding contact via.

Claim 73 (new): A method of forming an integrated circuit, as defined in claim 57, wherein between the ferroelectric device level and the transistor isolation layer is free of any interposing metal level.

Claim 74 (new): A method of forming an integrated circuit, as defined in claim 57, wherein throughout the ferroelectric isolation layer each ferroelectric isolation layer via is laterally sized larger than the corresponding contact via.